MULTI-BIT DATA TRANSMISSION ACROSS ASYNCHRONOUS TIME DOMAINS

ABSTRACT OF THE DISCLOSURE

A method and apparatus is provided for transmitting multi-bit data across asynchronous time domains. In one embodiment, the apparatus includes a first delay circuit to generate a selector signal based upon an input reference signal of a first time domain, a second delay circuit to generate a delayed data signal based upon an input data signal, and selection logic coupled to the first and second delay circuits to select one of the data signal and the delayed data signal based upon the state of the selector signal in accordance with an input clock signal of a second time domain, such that at any given sampling point of the input clock signal, the selector signal indicates valid data.